Charge Transport and Electroluminescence in PECVD Grown Silicon-Nanocrystals-Based LEDs

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[*]*Abstract* – **Electrical carrier injection into PECVD grown silicon-nanocrystals-based LEDs was examined by I-V, C-V, and impedance measurements. Electroluminescence was measured as a function of gate AC frequency. The correlations between conduction mechanism and electroluminescence are discussed.**

I. Introduction

In spite of the recent progress in silicon photonics we lack of an efficient Si-based light emitting device (LED) that will operate at low voltages being compatible with the standard CMOS technology [1]. Nanocrystalline silicon (nc-Si) is a way to achieve visible light emission from silicon with a good efficiency. Unfortunately, many difficulties are encountered to inject electrical charges into nc-Si due to the composite nature of the material. At present, Si-based electroluminescent devices operate with low efficiencies and at high voltages (above 5 V) at which the impact ionization mechanism dominates the generation of electron-hole pairs. Our research efforts are aimed at the realization of a device that will operate at low voltages under bipolar charge injection into nanocrystals.

Here we want to focus on the conduction mechanism and charge injection in silicon-nanocrystals-based LEDs grown by Plasma Enhanced Chemical Vapour Deposition (PECVD), a VLSI-compatible technique. We will look at the correlations between conduction mechanism and electroluminescence.

II. Experimental

The device structure is like a MOS capacitor where a PECVD deposited and annealed silicon rich oxide (SRO) or silicon-rich oxy-nitride (SRON) was used as gate dielectrics. The ratio between SiH_4, N_2O, and NH_3 was varied to control the excess amount of both Si and N in the SiO_2 matrix. The gate was formed by 30 nm thick layer of n-type in-situ doped poly-silicon, while 500 nm thick layer of Al (1% Si) is used to connect the gate area of $3.14 \cdot 10^{-8}$ m^2 with the bonding pad. The poly-Si is covered by an anti-reflective coating formed of a 50 nm thick Si_3N_4 layer and a 120 nm thick SiO_2 layer to improve light extraction. Wet oxidation was performed at 1050 °C for 1 hour to grow both 480 nm thick field oxide (for active area isolation) and Si nanocrystals in the gate dielectric. The thickness of the SRO layer was around 50 nm for all devices, which was controlled by both profilometer and Variable Angle Spectroscopic Ellipsometry (VASE). The substrate was p-type (100) Si with the resistivity of 12-18 Ω·cm.

The current-voltage (I-V) characteristics were obtained using HP 4145A semiconductor parameter analyzer. The capacitance-voltage (C-V) measurements were done with HP 4284A precision LCR meter. A 2 meter long extension cable was used. The open and short circuit corrections were performed according to the operation manual. The alternating current (AC) signal voltage level was 50 mV. The C-V data were collected at two frequencies 1 and 100 kHz. The delay time in the I-V and C-V measurements was one second to balance measurement speed and measurement integrity. The scanning voltage step was 100 mV. The electroluminescence (EL) was collected with a Spectra-Pro 2300i Monochromator coupled with a CCD camera. The monochromator was set to the zero order configuration to measure the emission integrated over the whole visible range. The total light intensity was then calculated by integrating the CCD signal over the illuminated pixels. The measurements were performed at room temperature in a dark room.

We prepared a control MOS device with the stoichiometric SiO_2 gate dielectric using PECVD technique and measured its I-V and C-V characteristics. Our C-V modeling shows a good agreement with the experimental data. The good agreement indicates that our control SiO_2 device has good MOS-structure properties, namely oxide layer is a good insulator, the oxide is free of charge, and planar interface Si/SiO_2 is free of electronic trap levels and space charge.

III. Results And Disscusion

A. *I-V and EL measurements*

We selected a high conductivity device for our I-V and EL measurements, so that appreciable currents could be measured even at low voltages. The device has the SRO layer with the Si content of 54 at. %. During the 1 hour long annealing at 1050 °C, large silicon nanocrystals (larger than 5 nm [2]) embedded into SiO_2 matrix were obtained. The average distance between nanocrystals was estimated in the order of few nanometres.

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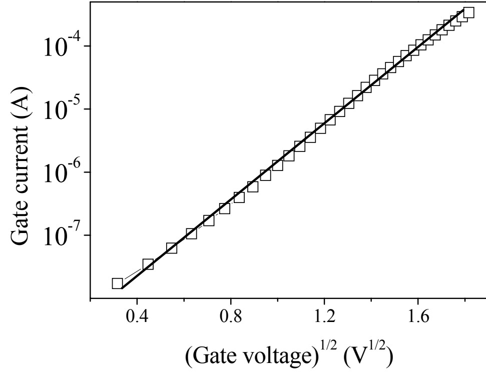

Fig. 1. The Schottky plot of the I-V characteristic of a device with the Si content of 54 at. % at low gate voltages.

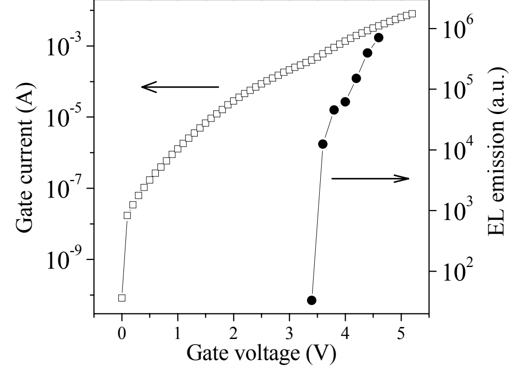

Fig. 2. I-V characteristic (empty squares) and EL emission (full circles) as a function of the gate voltage. The device is SRO with the Si content of 54 at.%. The EL emission is integrated over the whole visible range.

The trap-assisted model fits well the electron tunnelling through the SRO layer. This tunnelling process is similar to the Schottky emission and it can become dominant over the direct tunnelling mechanism at low field strengths [3]. Depending on the temperature and the thickness of the barrier, either of these two processes can dominate. The Schottky emission dominates at low voltages and the direct tunnelling at higher voltages. Furthermore, the thicker the film and the smaller the barrier height, the larger is the voltage range over which the Schottky mechanism dominates [4]. The J-V characteristic for the Schottky emission is given by (1)

$$J \propto T^2 \exp\left(a\sqrt{V}/T - q\left(\Phi_B/(kT)\right)\right). \quad (1)$$

Here $a = \sqrt{q/(4\pi\varepsilon_i d)}$, q is the unit charge, d is the oxide thickness, ε_i is the substrate permittivity, k is Boltzmann's constant, T is the absolute temperature, Φ_B is the barrier height, and V is the gate voltage [5]. Fig. 1 shows the I-V characteristic of the device with the Si content of 54 at. % at low gate voltages. The data follows a straight line in the Schottky plot, which is the logarithm of current as a function of the square root of voltage. This is in accordance with the trap-assisted conduction mechanism that we discussed above.

Fig. 2 shows the EL emission as a function of the gate voltage. The voltage range has been extended with respect to the previous graph to the values where the impact ionization mechanism is activated. The EL intensity declines when the gate voltage decreases and it steeply drops when the voltage reaches the value of 3.4V, the value that corresponds to the barrier height at Si/SiO_2 interface.

The SRO layer as depicted by these experimental evidences is quite articulated. The nanocrystals are not well insulated from each other because the oxide matrix is distorted and many defect states surround the nanocrystal interface. In these conditions the conduction of electrons preferentially occurs through the defects and the Si nanocrystals are left out of the conductive paths. When the bands are sufficiently bended by the external field, the electrons can be injected into the conduction band of the oxide and they can release their energy by impact ionization. In the case of hot electrons, the injection into the nanocrystals is favoured because they minimize their energy by falling down into the nc-Si conduction band. The EL observed in the Fig. 2 originates from the recombination of the electron-hole pairs generated by impact ionization in the nc-Si.

B. C-V Measurements

We undertook a few high-frequency C-V and impedance measurements in order to clarify the trap-assisted charge transport model described in the previous section.

Fig. 3 shows the C-V characteristics for both SRO and SRON devices with the same silicon content of 48 at. %. The measurements were performed in a progressive cycling manner around zero biasing voltage that is sketched in the inset. The cycling starts at zero voltage and the device was first swept to -1V and then to +1V. In the subsequent cycling scans the absolute value of the biasing voltage increases by 1V. C-V hysteresis was found at ±1V cycle (a "scanning" voltage value is 1V) that becomes wider and wider until the scanning voltage reaches the value of 3 V. The C-V curves have a distorted shoulder-like shape. We attribute this shoulder to the trapping of charges at the nc-Si/SiO_2 interface or near the interface region [6-8]. The hysteresis is counterclockwise that is the indication of the net positive charge accumulated in the oxide layer. We did not observe a dependence of the hysteresis on the AC signal frequency.

The shift in the flat-band voltage and the hysteresis loop width is much larger for SRON device than for SRO one, namely it is 1.5V versus 0.75V in the latter case. The SRON device has around 3 at. % of nitrogen in excess with respect to the SRO device. Nitrogen in the oxide matrix creates new sites for charge trapping, which is due to an excess of SiN dangling bonds. The C-V hysteresis width should scale linearly with the integrated photoluminescence (PL) intensity because both C-V hysteresis width and PL intensity depend on the nanocrystal density [9]. However, this does not hold for our measurements: PL intensity value for SRON device is about the same as the value for SRO device [2].

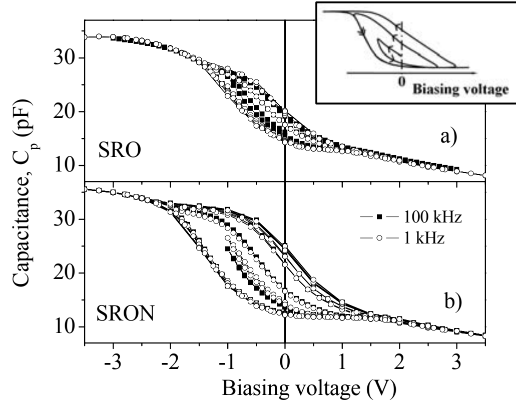

Fig. 3. C-V hysteresis in MOS structure with a) SRO layer and b) SRON layer measured in a cycling manner around zero voltage. Voltage cycling is sketched in the inset.

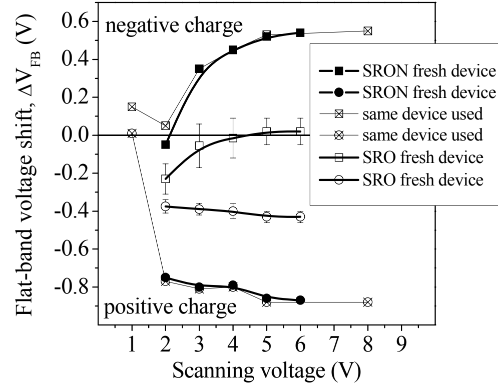

Fig. 4. The shift in the flat-band voltage as a function of scanning voltage; squares – scanning from the inversion region to the accumulation region, and circles – scanning from the accumulation to inversion region.

This indicates that the observed C-V hysteresis is due to the trapping and de-trapping of electrons at nc-Si/SiO_2 interfaces rather than charging and discharging of silicon nanocrystals itself. The net positive charge observed in the C-V measurement is due to positive charges trapped in the oxide layer.

The flat-band capacitance of our MOS structures is around 27 pF and 29 pF for SRO and SRON devices, respectively. Using these values, we calculated a shift in the flat-band voltage, ΔV_{FB}, which the measured C-V curves have with respect to the theoretical value that is around -0.9 V. The results are demonstrated in the Fig. 4. Zero value of the flat-band voltage shift corresponds to the neutral state of the oxide, while positive and negative values indicate the accumulation of net negative and positive charges, respectively. Both SRO and SRON fresh devices have some positive charge trapped in the oxide matrix. Scanning from the deep depletion region to the accumulation region brings about the neutral state for the SRO device and negative charge trapping in the SRON device with the scanning voltage above 2V. When the same device is scanned twice being scanned first to some high positive voltage (the reverse bias) it shows the presence of some negative charge at the scanning voltage of 1V. Further voltage scanning charges and discharges the device in a reversible manner. It is important that charged (squares) and discharged (circles) branches in Fig. 4 demonstrate different voltage dependencies. Higher positive voltages are needed to reach the neutral (negative) oxide state, while the positive oxide state is almost voltage independent. This indicates a different origin of the positive and negative charges in the oxide layer: the positive charge is the charge trapped within the nc-Si/SiO_2 interface, while the negative charge is due to injected electrons captured in Si nanocrystals or the same nc-Si/SiO_2 interface.

We estimated the trap density from the following formula $N_t = C_{ox}\Delta V / qA_G$. Here N_t is the trap density, A_G is the gate area, C_{ox} is the oxide capacitance, and ΔV is the hysteresis width. The estimates are $5 \cdot 10^{11}$ cm^{-2} and 10^{12} cm^{-2} for SRO and SRON devices, respectively.

IV. CONCLUSIONS

Silicon nanocrystals based LEDs were prepared by PECVD. Electrical charge injection and charge trapping effects in the nc-Si LEDs are discussed. The EL emission originates from the recombination of the electron-hole pairs generated by the impact ionization of silicon. The lack of the EL emission at low gate voltages is attributed to the trap-assisted charge tunneling. The presence of interface charge traps is supported by the C-V measurements. The charging and discharging effects in nc-Si-based LEDs were analyzed.

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