

Deep-UV Lithography Fabrication of Slot Waveguides and Sandwiched Waveguides for Nonlinear Applications

E. JORDANA, J.-M. FEDELI, P. LYAN, J.P. COLONNA, P. GAUTIER (1),
N. DALDOSSO, L. PAVESI (2),

Y. LEBOUR, P. PELLEGRINO, B. GARRIDO, (3)

1) CEA-Léti, MINATEC, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France,
emmanuel.jordana@cea.fr

2) Laboratorio Nanoscienze, Dipartimento di Fisica, Università di Trento, via Sommarive 14, I-38050 Povo, Trento, Italy, daldosso@science.unitn.it

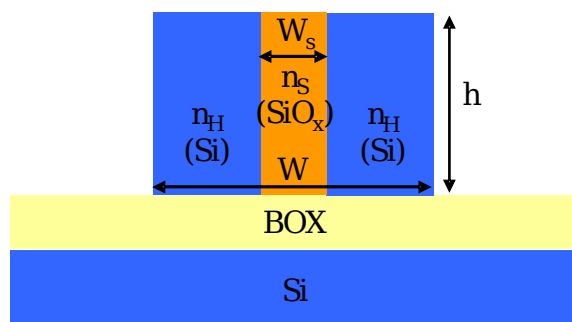
3) EME, Departament d'Electrònica, Universitat de Barcelona, Martí i Franquès 1, 08028 Barcelona, Spain, blas@el.ub.es

Abstract: Associated to silicon nanocrystals, slot waveguides are promising components for the fabrication of fast optical switches. We report here on the fabrication of slot waveguides with industrial microelectronic tools, especially DUV lithography. The filling of slot waveguides with silicon nanocrystals within SiO_2 by PECVD and LPCVD deposition results in almost filled waveguides owing to incorrect silicon etching profiles. We also report on slot waveguide alternative structure: the sandwiched waveguide. This structure eliminates the slot filling step and allows slot thickness as thin as desired. The association of silicon nanocrystals and slot waveguides, if used in a Mach-Zender Interferometer structure, will pave the way to compact all-optical XOR logic gates entirely fabricated with microelectronics tools.

Introduction

Using silicon as a photonic material is of great interest since this would allow a coherent continuity between electrical and optical circuits since its full CMOS compatibility. Moreover the Si/SiO₂ system is very well known chemically, thermally and mechanically. Furthermore it would be possible to develop low cost and all-optical communication networks without bottlenecks induced by electrical/optical converters. Passive devices (filters, couplers, multiplexers...) have already been demonstrated using silicon-based waveguides and materials exhibiting nonlinear optical properties. Contrary to bulk silicon which presents poor nonlinear properties, silicon nanocrystals embedded in SiO₂ are considered as a very promising material for nonlinear applications as its Kerr coefficient was reported to be in the range of two and four orders of magnitude higher than that of bulk Si and SiO₂, respectively ($n_2 \sim 10^{-16} \text{m}^2/\text{W}$) [1]. Fabricated by high temperature annealing of LPCVD or PECVD deposition of non-stoichiometric SiO_x layers, nonlinear properties can be tuned according to nanocrystallites size and density [2].

As silicon nanocrystals within SiO₂ have a relatively low refractive index, their use in conventional strip waveguides would result in a large cross-section and weak light confinement. So new waveguide architecture, using E-field discontinuity at the interfaces and where light propagates mostly in the low-index medium, has been proposed: the slot waveguide [3]. It is based on the fabrication of a 100nm-150nm (W_s) wide slot in a monocrystalline silicon waveguide with a width (W) of approximately 500nm and a height (h) of 200-300nm (Fig. 1).



For nonlinear applications the slot is filled with SiO_x . After high temperature annealing all the structures are finally covered by stoichiometric SiO_2 .

Fig. 1: View of a slot waveguide ($W_s=100\text{-}150\text{nm}$, $h=200\text{-}300\text{nm}$, $W=500\text{nm}$, $n_H \leftrightarrow$ high index medium : silicon, $n_S \leftrightarrow$ small index medium : silicon nanocrystals within SiO_2).

Strong index contrast and geometrical confinement enables fabrication of miniaturized components enabling optical logic gates with reduced optical power and dimensions.

Enhancement of the efficiency of nonlinear processes by a factor $(c/v_G)^2$ is also possible by using slow wave structures concept reducing the group velocity of the light in resonant structures, like slot waveguide-based ring resonators. Slot waveguides and slot waveguide-based ring resonators have already been fabricated using electron-beam lithography but, due to low temperature, PECVD SiO_2 deposition did not fill the slot [4]. Furthermore electron-beam lithography is not compatible with CMOS mass-manufacturing. So the aim was to demonstrate the faisability of slot waveguides with microelectronics tool for cost reduction of the associated optical systems. Using Deep-UV lithography and conventional tools for deposition and etching, two different concepts of slot waveguides are demonstrated.

Slot waveguides defined with DUV lithography

DUV lithography either at 248nm or 193nm on ASML equipment were used for the purpose of future mass manufacturing. Starting on wafers with 380nm silicon thickness, 150nm thick SiO_2 was deposited as hard mask. After definition of the patterns and hard mask etching, silicon was etched to the buried oxide. Finally a non-stoichiometric SiO_x layer was deposited by LPCVD or PECVD and annealed at 1100°C in a RTP furnace to induce silicon nanocrystals formation. The slots are 120, 140, 160, 180 and 200nm wide with different guide widths of 500, 520, 540 and 560nm.

Deep-UV 248nm lithography on ASM300 has been successfully used to achieve 120nm slot waveguides. Slot waveguide definition increases with the exposition dose but slot definition is insufficient and rough. Some slots waveguides were successfully defined but the process margins were too low for a reliable fabrication as critical dimensions are above Deep-UV 248nm lithography limits.

For mass manufacturing with acceptable fabrication margins, Deep-UV 193nm lithography on ASM1100 scanner was experimented with different exposition doses. Slot waveguides with slots as thin as 120 and 100nm were successfully defined with high reproducibility (Fig 2). In order to achieve silicon etching, HBr chemistry has been chosen since HBr plasma provides excellent anisotropic etching with a very good selectivity to the oxide. However the filling of a trench with a high form factor is a challenge that we try to ease by giving some slope to the silicon edges.

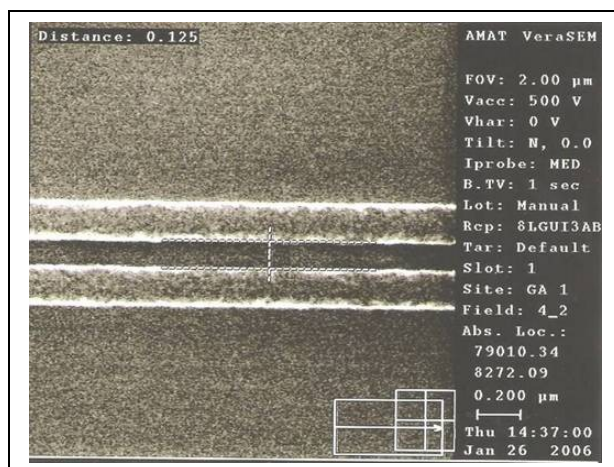


Fig 2: 193nm DUV lithography of slot waveguide

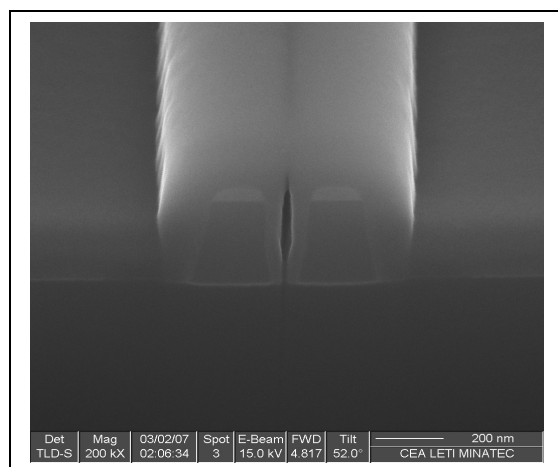


Fig.3: SEM cross-section view of a 500nm wide slot waveguide ($W_s=120\text{nm}$)

just after SiO_x cladding deposition by LPCVD

On Fig. 3 is reported a FIB-SEM cross-section view of a 500nm wide slot waveguide with a 120nm wide slot which has been covered with SiO_x LPCVD. It is obvious that slot waveguide is not filled even if LPCVD deposition shows a better filling ability than PECVD deposition (not showed) since it is more conformal. To reduce even more the steepness for the silicon waveguide, we etch the silicon layer using only the resist. We could not achieve ever a good filling of the slot with SiO_x.

To relax the filling constraint, we inverted the process in order to obtain slot waveguide: the concept is to define the slots first as a wall and grow the silicon in contact with the slots. Starting with SOI wafers (50nm Si / 2µm BOX), 300nm SiO_x was deposited and annealed at high temperature. 60nm Si₃N₄ was deposited as CMP stop layer, followed by 150nm amorphous carbon layer as hard mask for SiO_x etching. After slots definition by DUV 193nm lithography and hard mask etching, SiO_x was etched down to the thin Si layer. Then after careful cleaning, Si epitaxy was achieved, followed by Si planarization by CMP down to Si₃N₄ layer. Finally a 500nm SiO₂ cladding layer is deposited on the whole structure.

The main advantage of this fabrication method is to avoid SiO_x deposition in slots which is unable to fill-in slots with SiO_x. However the difficulty comes from the SiO_x etching due to the inhomogeneous nature of the material. As can be seen on figure 4 representing a SEM cross-section of a etched SiO_x structure just after Si epitaxy, the edges of SiO_x are steep and smooth enough to allow the epitaxy of monocrystalline Si.

Sandwiched waveguides fabrication

In order to reduce processing difficulties encountered in slot filling or SiO_x etching, an alternative process was developed by turning the slot by 90°. On 200mm SOI wafers with 205nm Si and 1µm BOX, SiO_x deposition was achieved with a thickness between 50nm and 120nm either by LPCVD or PECVD. The silicon nanocrystals we formed after 1000°C RTP annealing in N₂ atmosphere. Then low loss hydrogenated amorphous silicon [5] was deposited followed by 300nm TEOS SiO₂ deposition acting as hard mask.

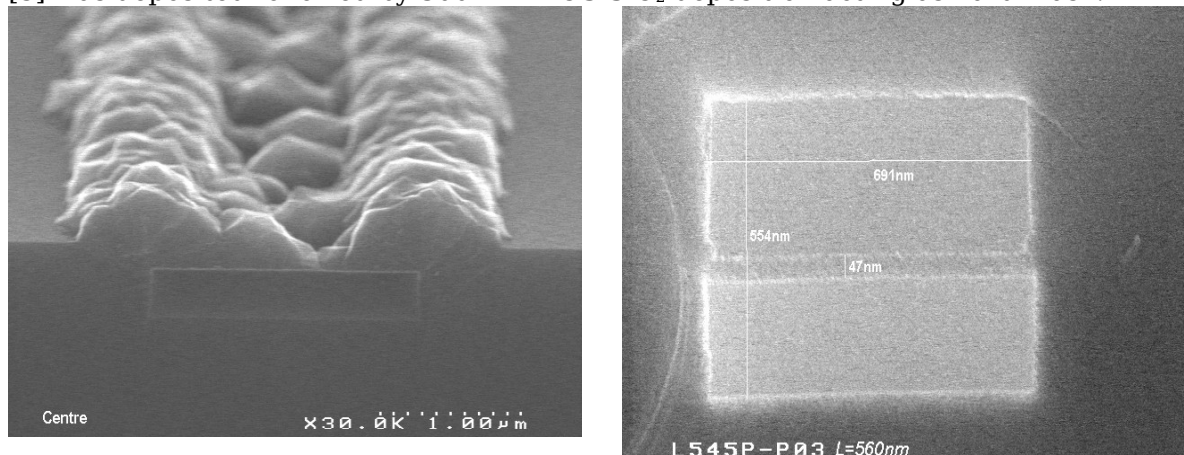
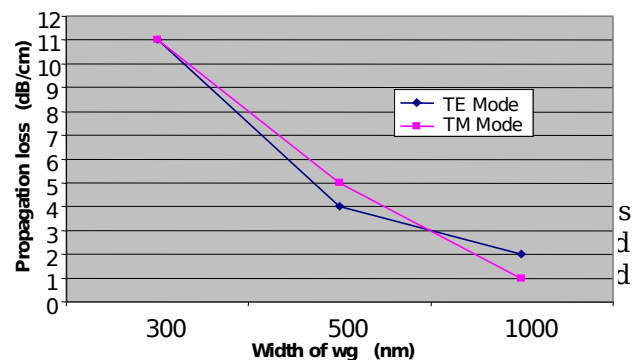


Fig. 4: SEM cross-section of a etched SiO_x structure just after Si epitaxy.

After 248nm Deep-UV lithography and hard mask etching (using a hard mask of silicon, SiO_x and monocrystalline silicon) oxide. Finally a SiO₂ TEOS cladding layer was deposited. Finally waveguides of 300 and 500nm width were

On figure 5 representing a cross section



of a typical waveguide, some imperfections can be observed as a notching effect: lateral etching of the amorphous silicon just above the SiO_x layer. Nevertheless, the thin SiO_x layer, obtained by LPCVD, leads to strong confinement of the light. Propagation losses of the waveguide reported in Fig. 6, were extracted by injecting light at 1550nm in a 1mm long waveguide for different widths and the output of this waveguide was monitored for TE and TM polarization. As low as 4dB/cm propagation losses were measured for the two polarizations on 500nm width waveguide.

Fig 6: Propagation losses of sandwich SiO_x waveguide

Conclusion

Different slot waveguides configurations using microelectronics industrial tools have been fabricated. Despite a successful DUV lithography and Si etching, the complete filling of the slot with SiO_x material either with PECVD or LPCVD could not be achieved. An inverted process is proposed starting with SiO_x etching. To reduce difficulties, an alternative process relying on low loss a-Si:H layer leads to the fabrication of sandwiched waveguides. With this process, SiO_x slots as thin as 10nm can be obtained, leading to an increase of the light confinement. The fabricated sandwiched waveguides exhibited propagation loss as low as 4dB/cm. These first results are thus the first step toward the low-cost CMOS compatible manufacturing of all optical silicon-based logic gates.

Acknowledgments

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