

Electrical conduction and electroluminescence in nanocrystalline silicon-based light emitting devices

S. Prezioso,¹ A. Anopchenko,^{1,a)} Z. Gaburro,¹ L. Pavesi,¹ G. Pucker,² L. Vanzetti,² and P. Bellutti²

¹Laboratorio di Nanoscienze, Dipartimento di Fisica, Università di Trento, Via. Sommarive 14, Povo, 38100 Trento, Italy

²Microtechnologies Laboratory, Fondazione Bruno Kessler, Via Sommarive 18, Povo, 38100 Trento, Italy

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Electrical transport and light emission properties of plasma-enhanced chemical vapor deposition grown light emitting devices (LEDs) based on nanocrystalline silicon have been studied. Various active layer compositions have been used. Electroluminescence and current-voltage measurements have been performed on metal-oxide-semiconductor structures. We found that Poole–Frenkel emission and trap-assisted tunneling between traps located at the nanocrystalline silicon interfaces are consistent with the measurements. The interface trap density was estimated. Its dependence on the composition of the active layer is discussed. We propose an equivalent electrical circuit model for the LED based on complex impedance measurements. Nanocrystalline silicon electroluminescence in the near infrared region is explained by hot-electron injection and impact ionization mechanism. It is concluded that the trap-assisted tunneling and charge trapping limit the external power efficiency of this kind of devices. © 2008 American Institute of Physics.

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I. INTRODUCTION

The silicon light emitting device (LED) is a very desirable component in silicon photonics.¹ Several physical and engineering solutions exist, which demonstrate an enhanced silicon emission in both infrared and visible regions.^{2–5} However, the device external or power efficiency remains low, and has still to be radically improved for practical silicon LED applications. One way to achieve high power efficiency is to use the quantum confinement effects in nanocrystalline silicon (nc-Si).¹ As a result, visible light emission in silicon becomes possible with high radiative recombination rates.

It is also very desirable to have devices compatible with the present industrial complementary metal-oxide-semiconductor (MOS) technology. This could be realized by embedding silicon nanocrystals into the silicon oxide matrix of a MOS device. The silicon nanocrystal composites could be grown by plasma-enhanced chemical vapor deposition (PECVD), for example, which is followed by a high temperature annealing.

The problem of charge injection arises as a result of embedding nanocrystals into the silicon oxide dielectric matrix. To obtain an efficient light emitter, balanced bipolar charge injection into the nanocrystals has to be realized. Good nanocrystal passivation and isolation have to be optimized with charge injected into the nanocrystals under low voltages. In principle, this could be possible when the thickness of the silicon oxide between the nanocrystals is reduced at a value that tunneling currents become important. Direct tunneling is a conduction mechanism that leads to large injected electrical currents at low applied voltages without leading to the oxide degradation. Present silicon LEDs work

under high voltages (above 5 V) at which unipolar Fowler–Nordheim tunneling is the main charge injection mechanism.^{5,6} We are aware of only one work that claimed the demonstration of the bipolar transport under 5 V in nanosilicon composite.⁷ The Fowler–Nordheim tunneling induces a positive charge in the silicon oxide and leads to its degradation.⁸ There is some discussion in literature about electroluminescence (EL) quenching due to charge trapping in nc-Si LED.⁹ On the other hand, in stoichiometric oxide based MOS devices and depending on the oxide thickness direct or trap-assisted tunneling (TAT) can dominate.¹⁰ The direct tunneling current is larger than the trap-assisted one for the oxide thickness thinner than 2.6 nm, where the main contribution to the direct tunneling current is from electrons that belong to the twofold degenerated valleys only.¹⁰

In this work we study nc-Si LED grown by PECVD and discuss its light emission characteristics. We will show how the electrical conductance and EL depend on the composition of the active layer. The electrical conduction mechanism will be analyzed and an equivalent electric circuit of the LED will be presented.

II. EXPERIMENT

A. Device fabrication

Different MOS-like capacitors were realized using either silicon rich oxides (SRO) or silicon-rich oxynitrides (SRON) deposited by PECVD as dielectric material. First, the active layer of the LED was deposited by PECVD on 4 in. Si substrates. The substrates were *p*-type (100) Si with the resistivity of 12–18 Ω cm. During PECVD deposition, the ratio among the precursor gasses (SiH₄, N₂O, and NH₃) was varied to control the excess amount of both Si and N in the SiO₂ matrix. The different deposited layers are identified by a

^{a)}Electronic mail: anopchenko@science.unitn.it.

TABLE I. Device structural, optical, and electrical characteristics.

Device	SRO thickness (nm)	Refractive index at 600 (nm)	Si content ^a (at. %)	O content ^a (at. %)	N content ^a (at. %)	SRO capacitance ^b (pF)	SRO dielectric constant
Γ 3	42 ± 4	2.49 ± 0.01	52	44	4	56 ± 1	8.5 ± 1.0
Γ 3N	32 ± 4	2.58 ± 0.01	54	38	8	88 ± 2	10.1 ± 1.5
Γ 10	50 ± 2	1.82 ± 0.01	48	47	5	34 ± 1	6.1 ± 0.4
Γ 10N	47 ± 2	1.81 ± 0.01	48	44	8	36 ± 1	6.1 ± 0.4
Γ 15	49 ± 2	1.69 ± 0.01	44	50	6	31 ± 1	5.5 ± 0.4

^aAtomic percentages of oxygen, nitrogen, and silicon were calculated from XPS measurements using atomic sensitivity factors.

^bThe electrical circuit capacitance values in the case of Γ 3 and Γ 3N devices.

symbol Γ , which is defined as the ratio between the N_2O and the SiH_4 fluxes used during the deposition process. Γ is inversely proportional to the Si content inside the oxide matrix. In addition, in order to evaluate the role of the N content, 40 SCCM (SCCM denotes cubic centimeter per minute at STP) of NH_3 were added in the deposition chamber during the deposition of a few SRON layers. In this case, the devices are labeled with an index “N” following the Γ value. The thickness of the SRO layers was around 50 nm for all devices (see Table I for details). After deposition, wet oxidation was performed at 1050 °C for 1 h to grow both 480 nm thick field oxide (for active area isolation) and Si nanocrystals in the gate dielectric. Then, the devices were processed by using a standard MOS process. The gate was formed with a semitransparent 30 nm thick layer of *n*-type *in situ* doped polysilicon. Different geometries were used for the metallization: a circular geometry with a ring-shaped metal line for emission study (LED) and a disk geometry entirely covered by the metal contact for electrical studies (capacitor). Metallization was done with a 500 nm thick layer of Al (1% Si), which is used to connect the gate area of $7.94 \times 10^{-8} \text{ m}^2$ in the LED (capacitor for electrical characterization has a gate area of $3.14 \times 10^{-8} \text{ m}^2$) with the bonding pad. In the LED geometry, the poly-Si is covered by an antireflective coating formed by a 50 nm thick Si_3N_4 layer and a 120 nm thick SiO_2 layer to improve light extraction. Figure 1 reports the schematic cross section and top view of the devices.

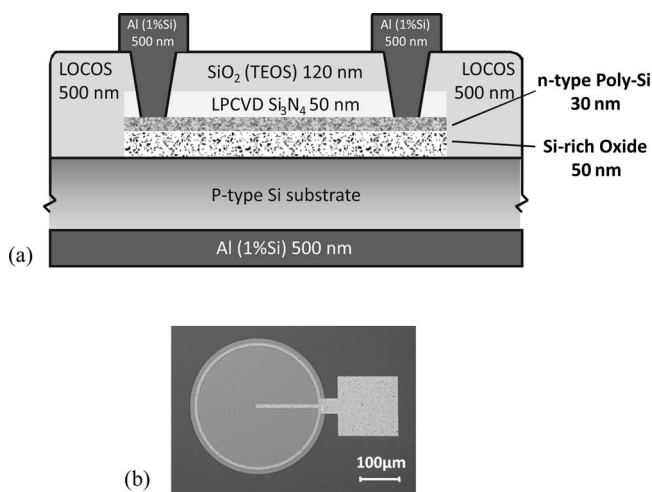


FIG. 1. The schematic cross section (a) and the top view of the devices (b).

A series of monitor wafers were prepared, which followed the process flow of the devices except for the definition of the device areas and contacts by photolithography and metallization. These monitor wafers were used for evaluation of layer thickness and structural analysis.

B. SRO and SRON characterization

Layer thickness after annealing was controlled by variable angle spectroscopic ellipsometry and depth profiling of sputter craters from secondary ion mass spectrometry (SIMS) on the monitor wafers. The SIMS measurement has been employed to obtain direct information about the thickness and the amount of excess silicon in the SRO layer. X-ray photoelectron spectroscopy (XPS) measurements were performed using a Scienta Esca-200 system equipped with a monochromatic $Al K\alpha$ (1486.6 eV) source. An overall energy resolution of 0.4 eV was routinely used. $Si 2p$, $O 1s$, $N 1s$, and $C 1s$ core levels were collected. All core level peak energies were referenced to the saturated hydrocarbon in $C 1s$ at 285.0 eV. The details of these analyses could be found elsewhere.¹¹ Here we summarize the general properties of the samples relevant for the interpretation of the electrical and EL properties, and discuss the structural changes introduced by the addition of NH_3 during the deposition. Photoluminescence (PL) measurements with the 488 nm Ar^+ laser have been performed to confirm the formation of nanocrystals in the SRO layer after the annealing.

The current-voltage (I - V) characteristics were obtained using the Agilent 4156C precision semiconductor parameter analyzer. The capacitance-voltage (C - V) measurements were done with HP 4284A precision LCR meter. A 2-m-long extension cable was used. The open and short circuit corrections were performed according to the operation manual. The alternating current (ac) signal voltage level was 50 mV. The C - V data were collected at two frequencies, 1 and 100 kHz. The delay time in the I - V and C - V measurements was 1 s to balance measurement speed and measurement integrity. The scanning voltage step was 100 mV. The impedance spectroscopy was utilized in the case of high-silicon excess, and hence high-conductive Γ 3 and Γ 3N devices, to obtain an equivalent electric circuit of the device and estimate the circuit capacitance. Impedance magnitude and phase were measured in the frequency range of 1–300 kHz. The bias swept from -4 to 4 V.

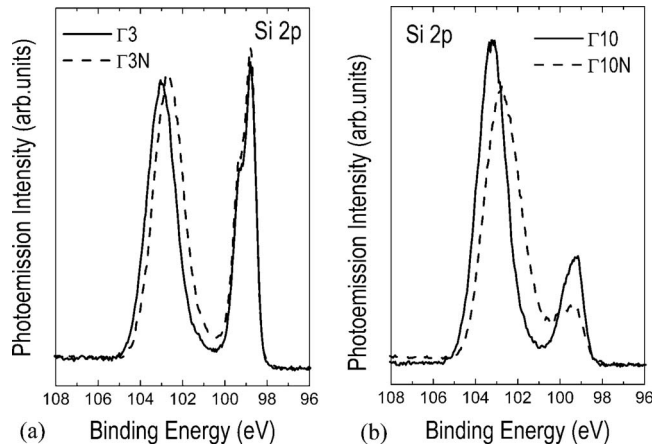


FIG. 2. High resolution XPS spectra of the Si $2p$ core levels of the samples $\Gamma 3$, $\Gamma 3N$ (a) and $\Gamma 10$, $\Gamma 10N$ (b).

The EL was collected with a Spectra-Pro 2300i monochromator coupled with a nitrogen cooled charge coupled device (CCD) camera. The monochromator was set to the zero order configuration to measure the emission integrated over the whole visible range. The total light intensity was then calculated by integrating the CCD camera signal over the illuminated pixels. The measurements were performed at room temperature in a dark room.

We prepared a control MOS device with the stoichiometric SiO_2 gate dielectric using PECVD technique and measured its I - V and C - V characteristics. Our C - V modeling shows a good agreement with the experimental data. The good agreement indicates that our control SiO_2 device has good MOS-structure properties, namely, oxide layer is a good insulator, the oxide is free from charge, and planar interface Si/SiO_2 is free from electronic trap levels and space charge.

III. RESULTS AND DISCUSSION

A. Nanocrystals formation: XPS and PL analyses

The XPS results for oxygen, nitrogen, and silicon concentrations in the measured samples are reported in Table I. The values (in atomic percentage) were calculated using atomic sensitivity factors. The XPS spectra of the Si $2p$ core level show that all the samples are phase separated in a Si(0) phase (either nanocrystalline or amorphous) and a silicon oxynitride matrix (with minor contribution of nitrogen with respect to oxygen). The amount of Si forming the silicon phase was estimated by comparing the intensity of the core level spectra with the ones of different oxides and bulk silicon. The Si-excess [percentage of Si(0) with respect to the total Si-content] for our samples has the following values: 11.2% $\Gamma 3$, 11.3% $\Gamma 3N$, 5.2% $\Gamma 10$, 3.5% $\Gamma 10N$, and 0.7% $\Gamma 15$. In Fig. 2 we show the Si $2p$ core levels of the samples $\Gamma 3$, $\Gamma 3N$, $\Gamma 10$, and $\Gamma 10N$. The Si $2p$ core level line shape shows a different chemical binding state for silicon and can be fitted into different components: SiO_2 (~ 104 eV), suboxides and silicon nitride (~ 103 – 102 eV), and Si(0) (~ 99 eV). Comparing the Si(0) component of $\Gamma 3$ and $\Gamma 3N$ with that of $\Gamma 10$ and $\Gamma 10N$, we note the decrease in intensity, which reflects the lower Si excess, and a change in the peak

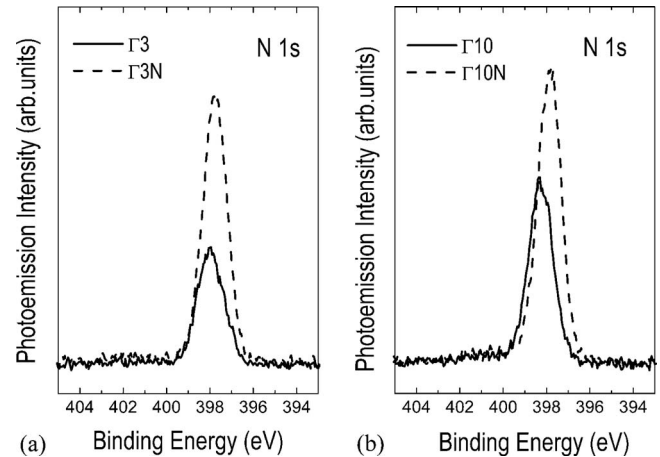


FIG. 3. High resolution XPS spectra of the N $1s$ core level of the samples $\Gamma 3$, $\Gamma 3N$ (a) and $\Gamma 10$, $\Gamma 10N$ (b).

shape. In the $\Gamma 3$ and $\Gamma 3N$ samples, the peak shape of the ~ 99 eV component shows the typical doublet structure known for crystalline Si. This doublet is less evident for the $\Gamma 10$ and $\Gamma 10N$ samples. This change in peak shape might be caused by the following two effects: (i) a transition from a more crystalline structure to an amorphous phase for the excess silicon with increasing Γ , or (ii) different bond lengths and angles for tiny nanocrystals caused by the strain near the interface. Moreover, the spectra in Fig. 2 show evidence of differences in bonding introduced by the NH_3 addition during the deposition. These differences in the bonding of nitrogen to oxygen and silicon are evident in the N $1s$ core level spectra as well. These spectra are shown in Fig. 3. It is clear that $\Gamma 3N$ and $\Gamma 10N$ samples have a larger overall nitrogen content than the corresponding $\Gamma 3$, $\Gamma 10$ samples (see also Table I). In addition the nitrogen bonding changes as well. This is evident from the shifts in the binding energy from 399 and 399.5 eV (samples $\Gamma 3$, $\Gamma 10$) to 398.5 eV (samples $\Gamma 3N$, $\Gamma 10N$). A comparison with the binding energies of nitrogen in Si_3N_4 shows that the ΓN samples have N $1s$ binding energies similar to those observed in Si_3N_4 . This means that nitrogen introduced in the form of NH_3 is mainly bonded to silicon [$\text{Si}-\text{N}(\text{Si})_2$].

The PL spectra of the various deposited layers are shown in Fig. 4. The PL spectra reflect the formation of nc-Si in

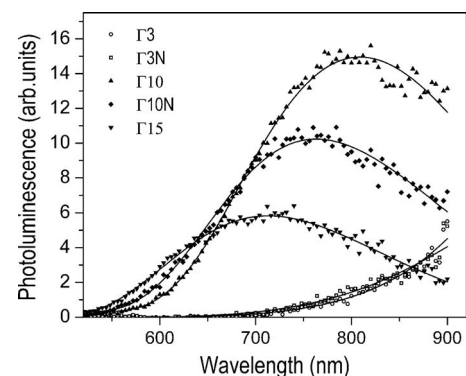


FIG. 4. PL spectra collected from the monitor wafers with Ar laser at 488 nm. Incident power was 50 mW. The spectra are normalized for spectrograph response. The devices are indicated in the figure legend.

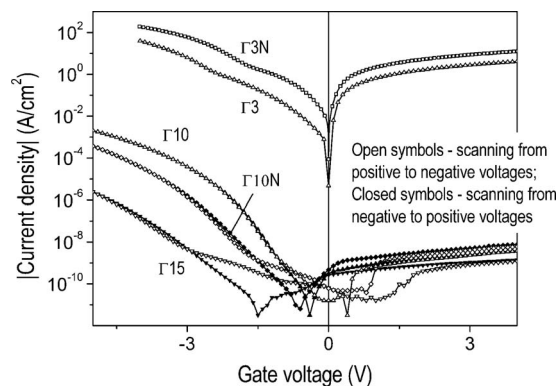


FIG. 5. Absolute value of MOS-LED gate current density as a function of applied gate voltage, I - V characteristics. Open symbols: scanning the MOS-LED from inversion to accumulation. Closed symbols: scanning from accumulation to inversion. Devices are marked.

SiO₂ matrix. It can be seen that when the Γ value is decreased (i.e., increasing the excess silicon content) the PL peak wavelength redshifts, indicating the formation of large nanocrystals. For the highest Γ value (Γ_{15}) the PL peak has been found at around 720 nm while for the lowest Γ value (Γ_3) the spectrum peaks at wavelengths longer than 900 nm. From the PL peak wavelength for high Γ values (Γ_{10} , Γ_{10N} , and Γ_{15}) the band gap can be estimated to fall in the range of 1.6–1.7 eV. On the other hand, for low Γ values the band gap of the nanocrystals is very close to that of bulk Si. It is noteworthy that PL peak intensity decreases in the following order: Γ_{10} , Γ_{10N} , and Γ_{15} in correspondence with the decrease in the Si excess estimated from the XPS analysis. Later we will show that the PL decrease is in opposite with an increase in charge storage capacity of the devices.

B. Conduction mechanism and equivalent electric circuit of the LED

The logarithm of the absolute value of current density across the oxide layer is shown in the Fig. 5 as a function of the applied gate voltage. The current-voltage (I - V) characteristics were collected scanning the gate voltage from positive to negative values and then in the opposite direction, from negative to positive voltages. The positive gate voltages correspond to a reverse bias. This is the gate polarity at which the depletion (inversion) layer is formed in the p -type silicon substrate. By analogy, the negative voltages correspond to a forward bias; the MOS device is in accumulation. The device conductivity increases to a large extent when the silicon content increases. The high- Γ devices (Γ_{10} , Γ_{10N} , and Γ_{15}) have been found to be less conductive as well as highly rectifying. The reverse currents in these devices were of the order of a few picoamperes whereas the forward currents were around few microamperes (at 5–10 V of biasing voltage). The I - V characteristics of the high- Γ devices resemble the I - V characteristic of a p - n junction diode, demonstrating an exponential dependence at low forward voltages and the effect of a series resistance at high forward voltages. The poor quality of the diode is reflected in an ideality factor (which gives the slope of forward-biased I - V in the straight region) that deviates significantly from unity, being smaller

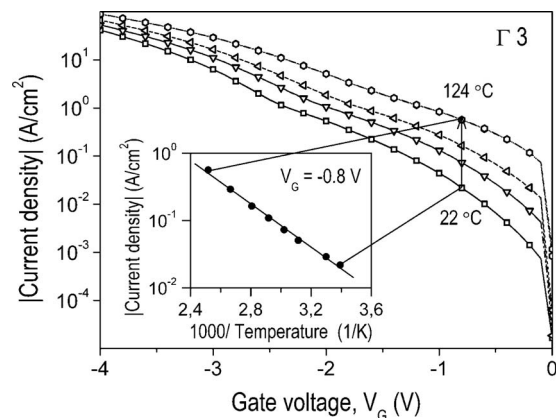


FIG. 6. Forward-bias I - V characteristics of Γ_3 device (shown in Fig. 5) at several elevated temperatures between 22 and 124 °C. Inset: Arrhenius plot of current density at the gate voltage value of -0.8 V.

for the low- Γ devices (Γ_{10}). The excess of nitrogen in the SRO layer decreases the conductivity. I - V hysteresis is observed for high- Γ devices (low silicon content). The hysteresis width is larger for the devices with lower conductivity although no hysteresis was observed for the low- Γ -devices with high conductivity (Γ_3 and Γ_{3N}). The hysteresis originates from the charge accumulated within the SRO layer. Positive charge is accumulated under the negative (forward) bias. Negative charge is accumulated under the positive (reverse) bias. As we will show later this accumulated charge is the charge trapped near the nanocrystal interfaces in the oxide layer. The low- Γ devices (Γ_3 and Γ_{3N}) are more conductive, and are a poor rectifier. The large reverse-bias current is due to the presence of electron traps (electron generation centers) in the nc-Si layer. The reverse current increases linearly with increasing bias. It is noteworthy that I - V characteristics for Γ_3 and Γ_{3N} devices under forward bias show a kink at the gate voltage around -2.4 and -1.6 V, respectively. We associate this kink with the energy barrier height at the interface between the silicon substrate and the active SRO layer, as detailed in the following:

To clarify the electric transport mechanism in our devices, we undertook some I - V experiments at several elevated temperatures. The I - V characteristics of Γ_3 device are shown in the Fig. 6. When temperature increases the device conductivity increases, demonstrating a larger increase at low gate voltages. This temperature increase is not consistent with any known tunneling mechanisms. It should be noticed that the change in the forward-bias voltage for a 10 °C temperature change is much larger than the typical -17.3 mV value for the ideal p - n junction diode. The increase obeys the Arrhenius law (see the inset), which is characteristic for a charge emission process. At voltages higher than the voltage value of the I - V kink, the temperature dependence is moderate, which points to a change in the conduction mechanism above and below the kink.

The electric field assisted thermal emission, also called Poole-Frenkel emission, is the most probable conduction mechanism at low electric fields. Poole-Frenkel emission is not a tunneling mechanism, and, in general, dominates at room temperature and moderate electric fields, and is governed by the following equation:¹²

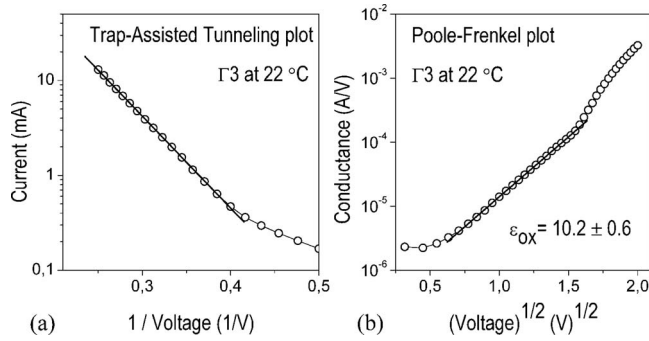


FIG. 7. Forward-bias I - V characteristic of $\Gamma 3$ device at 22 °C (the same as shown in Figs. 5 and 6). Left (a): TAT plot for the high-voltage region (above the kink). Right (b): the Poole-Frenkel plot showing a straight-line region at moderate voltages. The dielectric constant value calculated from the straight-line fit is 10.2 ± 0.6 .

$$I_{\text{PF}} \propto V \exp[-(q/rkT)(\phi_t - \sqrt{qV/d\pi\epsilon})]. \quad (1)$$

Here q is the unit charge, d is the oxide thickness, ϵ is the oxide permittivity, k is the Boltzmann's constant, T is the absolute temperature, ϕ_t is the trap energy level, V is the gate voltage, and r is a parameter ranging from 1 to 2 depending on the position of the Fermi level. Electron emission could occur through interface trap states. The interface trap states are probably located at the nc-Si interfaces, as we will show later. For a trap to experience the Poole-Frenkel effect, it must be neutral when filled and positive when empty.¹² The slope of the plot of $\log(I/V)$ versus $V^{1/2}$, which is also called Poole-Frenkel plot, will yield the dielectric constant of the device under test (the flatband voltage and surface potential are neglected being small). Figure 7 shows the Poole-Frenkel plot of the $\Gamma 3$ device at 22 °C, where a linear variation can be identified in the intermediated applied field. A linear regression through the data points gives a dielectric constant of 10.2 ± 0.6 , which is a good estimate for $\Gamma 3$ nanocrystal composite and agrees well with the value obtained from C - V measurements, as we will show later. The Fig. 7 shows also the high-voltage part of the same I - V characteristic, which is plotted in the so-called TAT plot, which is $\log(I)$ versus reciprocal voltage. The TAT current is governed by the following equation at high electric fields:¹³

$$I_{\text{TAT}} \propto \exp\left(-\frac{8\pi d\sqrt{2qm^*}}{3hV}\phi_t^{3/2}\right). \quad (2)$$

Here m^* is the electron effective mass in the SRO layer, and h is Planck's constant. A straight-line dependence is observed indicating a TAT of electrical charges under forward bias above the kink voltage of 2.4 V. This is the tunneling mechanism in which electrons from the gate electrode are able to tunnel directly into the nc-Si/SiO₂ interface trap states and then to tunnel into the silicon substrate.

To gain more insights into the electrical transport in our devices we derived an equivalent electrical circuit of the LED using impedance spectroscopy experiments. The complex impedance of $\Gamma 3$ and $\Gamma 3\text{N}$ device was measured in a broad frequency range and plotted in the log-impedance plot (Fig. 8) also called Nyquist or Cole-Cole plot. The lines through the data points are nonlinear least-squares fits, which

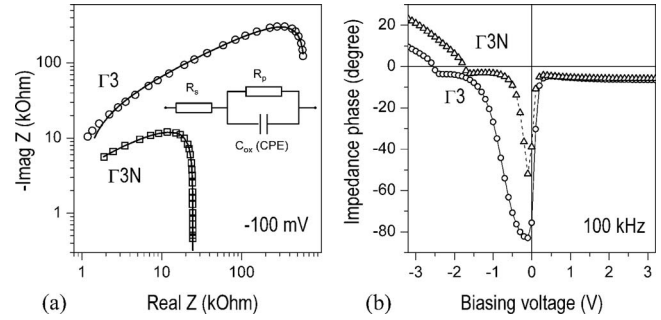


FIG. 8. Left: (a) Log-complex impedance plot for $\Gamma 3$ and $\Gamma 3\text{N}$ devices. The small-signal frequency spans the range of 1–300 kHz. The gate voltage is -100 mV. The inset shows an equivalent electrical circuit model for the LED (CPE stands for the constant phase element). Right: (b) The complex impedance phase as a function of the gate biasing voltage at the small-signal frequency of 100 kHz.

model the equivalent circuit shown in the inset. The fit parameters for series and parallel resistances of the $\Gamma 3$ device are $992 \pm 138 \Omega$ and $622 \pm 2 \text{ k}\Omega$, respectively, and $449 \pm 29 \Omega$ and $24.1 \pm 0.1 \text{ k}\Omega$ for the $\Gamma 3\text{N}$ device. The circuit capacitance values are listed in Table I. The circuit was derived for the gate voltages bracketing zero bias. The equivalent circuit resembles a small-signal equivalent circuit of the forward-biased p - n junction diode in which the circuit capacitance is the parallel combination of the junction and diffusion capacitances. The diffusion capacitance is the change in the stored minority carrier charge beyond the space charge region, which is alternately being charged and discharged through the junction as the voltage across the junction changes. The junction or depletion layer capacitance is normally much smaller than the diffusion capacitance and might be neglected.

As the gate bias increases (being forward or reverse) the conductivities of the $\Gamma 3$ and $\Gamma 3\text{N}$ device increase very rapidly and the equivalent circuit, which was described above, is no longer valid. The impedance phase as a function of the gate bias voltage is shown in the Fig. 8 at the fixed driving frequency of 100 kHz. As the forward voltage increases, the impedance phase decreases from around -90° (capacitive) to around -5° , and its derivative has a discontinuity at the kink voltage. Then, shortly after this, the phase becomes positive (inductive). This indicates that a larger amount of charges is able to tunnel through the oxide layer without being trapped.¹⁴ It is noteworthy that the bulk silicon edge emission was collected under these voltages (above the kink). The electrons tunnel through the oxide layer and ionize the silicon substrate where radiative recombinations inefficiently take place.

C. Charge trapping: Capacitance-voltage experiments

We undertook some high-frequency C - V measurements in order to clarify the trap-assisted charge transport model described above. Figure 9 shows the C - V characteristics for $\Gamma 10$, $\Gamma 10\text{N}$, and $\Gamma 15$ devices. The measurements were performed in a progressive cycling manner around zero biasing voltage. The cycling starts at zero voltage and the device was first swept to -1 and then to $+1$ V. In the subsequent cycling scans the absolute value of the biasing voltage increases by 1

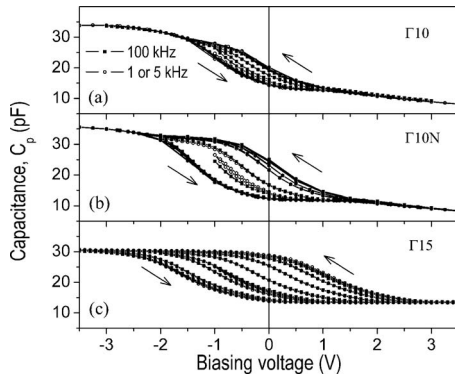


FIG. 9. The hysteresis of capacitance-voltage characteristics for the high- Γ devices: $\Gamma 10$ (a), $\Gamma 10N$ (b), and $\Gamma 15$ (c). The small-signal frequency was 1 (or 5) and 100 kHz. The arrows indicate the scanning direction.

V. C - V hysteresis was found at ± 1 V cycle (a “scanning” voltage value is 1 V) and became wider and wider until the scanning voltage reaches the value of 6 V. The C - V curves have a distorted shoulderlike shape, which is more evident in the case of $\Gamma 10$ device. This shoulder might be attributed to the mechanism of charge trapping at the nc-Si/SiO₂ interface or near the interface region.^{15–17} There is another interpretation of the shoulder. It might be linked to the mechanism of charge tunneling into the nanocrystals, which is similar to the observations on quantum dots in compound semiconductors.^{15,18} The hysteresis is counterclockwise (the arrows in the Fig. 9 point at the voltage scanning direction), that is the indication of the net positive charge accumulated in the oxide layer. We did not observe any dependence of the C - V characteristic on the small-signal ac frequency. We attribute this to a low density of the interface states at the SRO/substrate interface.¹⁹

The C - V hysteresis correlates very well with the hysteresis observed in the I - V characteristic. Its width is larger for the high- Γ devices. The shift in the flatband voltage and the hysteresis width is larger for $\Gamma 10N$ device than for $\Gamma 10$ one, namely, it is 1.5 versus 0.75 V in the latter case. The $\Gamma 10N$ device has around 3 at. % of nitrogen in excess with respect to the $\Gamma 10$ device (see Table I). The excess of nitrogen in the oxide matrix, which was introduced in the form of NH₃, slows down the formation of the nanocrystals. Nitrogen is bonded differently when deposited using NH₃ than nitrogen originating from N₂O which might be bonded to oxygen forming an O–N bond. In $\Gamma 3N$ and $\Gamma 10N$ devices nitrogen is threefold bonded to silicon as in Si₃N₄. This conclusion is derived from our XPS data analysis. Nitrogen tends to migrate to nc-Si interface where it is bonded to silicon and where it works as a diffusion barrier for oxygen.²⁰ This slows down the nanocrystal formation and creates interface trap states, which are due to the excess of Si–N dangling bonds.

The C - V hysteresis width should scale linearly with the integrated PL intensity because both C - V hysteresis width and PL intensity depend on the nanocrystal density.²¹ However, this does not hold for our measurements. The PL intensity values are in a reverse relation to the hysteresis width (Fig. 4). PL peak position for $\Gamma 15$ is blueshifted with respect to $\Gamma 10$, which means that nanocrystals in $\Gamma 15$ are smaller than in $\Gamma 10$. The same holds for $\Gamma 10$ and $\Gamma 10N$ devices, as

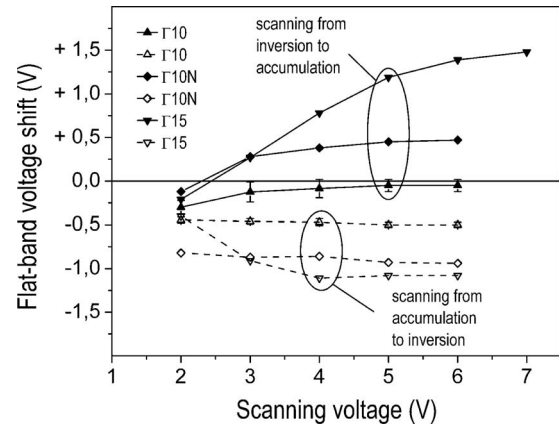


FIG. 10. The flatband voltage shift as a function of the scanning voltage for the C - V measurements shown in the Fig. 9. Closed symbols: negative charge branches, open symbols: positive charge branches. See the text for details.

confirmed by our XPS analysis. Taking this fact into account, the interface to volume ratio is increasing when Γ increases and hence the interface trap density will increase too. The smaller are the nanocrystals (the PL peak blueshift is more pronounced) the larger is the hysteresis width.

Estimating the flatband capacitance of our MOS structures, we calculated a shift in the flatband voltage, ΔV_{FB} , with respect to the theoretical flatband voltage, which is around -0.9 V. The results are shown in the Fig. 10. A zero value of the flatband voltage shift corresponds to the neutral state of the oxide, while positive and negative values indicate the accumulation of net negative and positive charges, respectively. All fresh devices show some positive charge accumulated in the oxide layer. The bias change from positive to negative values (inversion to accumulation) leads to the negative charging of the oxide (electrons injection). Scanning in the opposite direction, from accumulation to inversion, charges the oxide positively. The positive and negative branches (open and closed symbols in Fig. 10, respectively) demonstrate different voltage dependencies for the $\Gamma 10$ and $\Gamma 10N$ devices. Scanning from inversion to accumulation (electrons injection) brings about the neutral state for the $\Gamma 10$ device and negative charge trapping for the $\Gamma 10N$ device under the scanning voltage above 2 V. Higher scanning voltages are needed to reach the neutral/negative oxide state (reverse bias), while the positive oxide state is almost voltage independent. This points to a different origin of the positive and negative charges in the oxide layer: the positive charge is the detrapped interface states at the nc-Si/SiO₂ interface, while the negative charge is due to injected electrons, which become trapped at the nc-Si/SiO₂ interface. The process of charge trapping/detrapping is reversible. In the case of $\Gamma 15$ device, the number of detrapped interface states and hence the net positive charge of the oxide increases when the forward-bias voltage increases. At the scanning voltage of 4 V the net positive charge saturates. It is noteworthy that $\Gamma 10N$ and $\Gamma 15$ have a larger capacity to trap injected electrons in excess with respect to the $\Gamma 10$ device.

To summarize, the observed C - V hysteresis is due to the trapping and detrapping of injected electrons at the nc-Si/SiO₂ interface rather than charging and discharging of

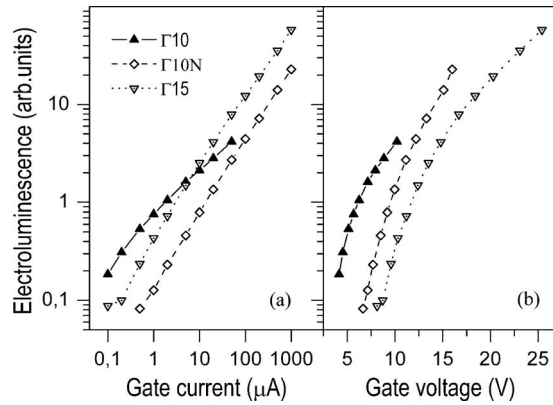


FIG. 11. Total integrated EL intensity as a function of the injected current (a) and applied gate voltage (b).

silicon nanocrystals itself. We estimated the trap density from the following formula: $N_t = C_{\text{ox}} \Delta V / qA_G$, where N_t is the trap density, A_G is the gate area, C_{ox} is the oxide capacitance, and ΔV is the hysteresis width. The estimates are 5×10^{11} and 10^{12} cm^{-2} for $\Gamma 10$ and $\Gamma 10N$ devices, respectively. The oxide capacitance value, C_{ox} , could be read directly from the measured C - V characteristic. These values for all devices are listed in the Table I. The oxide capacitance values allow us to estimate the oxide dielectric constant (see the Table I). The dielectric constant value for the $\Gamma 3$ device agrees well with the value obtained from the Poole–Frenkel model, which supports our model for trap-assisted electrical conduction.

D. Electroluminescence

Figure 11 shows the integrated EL as a function of injected current and gate voltage. No EL emission from nanocrystals was recorded for low- Γ devices, $\Gamma 3$ and $\Gamma 3N$, where PF and TAT are the main conduction mechanisms below and above the kink voltage, respectively. Only silicon bulk edge emission is present in these devices at the applied voltages above the kink value, when electrons are injected directly into the oxide conduction band and, being accelerated through the oxide layer, gain sufficient energy to generate electron-hole pairs in the silicon substrate. It is clear from Fig. 11 that the $\Gamma 10$ device shows the highest external power efficiency. At the same injected current the $\Gamma 10$ device shows the largest emission at the lowest applied voltage. The power efficiency value was conservatively estimated to be $2 \times 10^{-4}\%$ (measured with a silicon photodiode placed a few millimeters above the device; no corrections for the collection geometry were taken into account). The lack of EL emission under low forward-bias voltages (injected currents, respectively) and the low value of the external power efficiency are attributed to the TAT that is larger in our devices than the direct tunneling. At high injected currents the EL intensity becomes a sublinear function of the current, because of an increase in the rate of nonradiative processes. At the current value of $10 \mu\text{A}$ the EL intensity from $\Gamma 15$ device becomes larger than the EL intensity from $\Gamma 10$ device. However, the gate voltages that provide this EL intensity are much higher for $\Gamma 15$ than for $\Gamma 10$. As a result, the EL spectra of $\Gamma 15$ are much broader having an emission

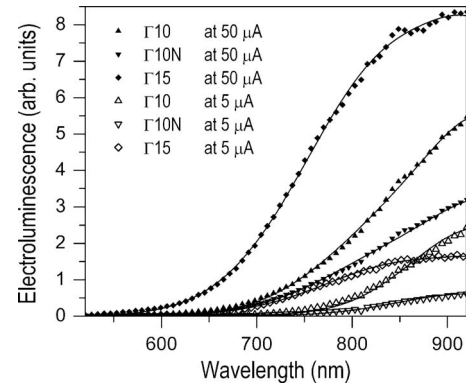


FIG. 12. EL spectra for high- Γ devices at the injected currents of 5 and 50 μA . The spectra are normalized for spectrograph response.

wing that extends to short wavelengths. The EL spectra collected at the injected currents of 5 and 50 μA are shown in the Fig. 12. The short-wavelength wing appears in the EL spectra of all devices at the current of 50 μA . This wing in EL emission might be attributed to the recombination of electron-hole pairs generated by hot electrons injected under high forward-bias voltages.²² A broad visible EL emission was also recorded under large reverse bias. This white EL emission from a reverse-biased silicon p - n junction has been already observed in similar nanostructures, and it has been well studied.²³ The clear differences between the PL and EL spectra provide another argument for the hot-electron mechanism of EL emission. The redshift in the EL spectrum of $\Gamma 10$ device at low injected currents can be also rationalized with the fact that only large nanocrystals could be luminescent as a result of rapid carrier tunneling.²⁴

IV. CONCLUSIONS

The nc-Si LEDs were grown by PECVD technique, and their electrical conduction mechanism and light emission were analyzed in detail. An equivalent electrical circuit for the LED was derived from the complex impedance experiment. The hysteresis effect found in the current-voltage and capacitance-voltage characteristics is explained by electron trapping at nc-Si/SiO₂ interface traps. The decrease in silicon content and/or increase in nitrogen content promote the formation of smaller nanocrystals and hence increase the nc-Si/SiO₂ interface trap density, which serve as electron generation-recombination centers. The absence of the EL emission under low forward-bias voltages might be attributed to a large number of interface trap states and TAT. The EL emission observed under forward-bias voltages above 5 V is due to the hot-electron injection and impact ionization. The TAT and charge trapping near the nc-Si interface are the main reason behind the low power efficiency of the devices.

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- ¹S. Ossicini, L. Pavesi, and F. Priolo, *Light Emitting Silicon for Micro-Photonics*, Springer Tracts in Modern Physics Vol. 194 (Springer-Verlag, Berlin, 2003).
- ²K. D. Hirschman, L. Tsybeskov, S. P. Duttagupta, and P. M. Fauchet, *Nature (London)* **384**, 338 (1996).
- ³W. L. Ng, M. A. Lourenco, R. M. Gwilliam, S. Ledain, G. Shao, and K. P. Homewood, *Nature (London)* **414**, 470 (2001); **410**, 192 (2001).
- ⁴M. A. Green, J. H. Zhao, A. H. Wang, P. J. Reece, and M. Gal, *Nature (London)* **412**, 805 (2001).
- ⁵R. J. Walters, G. I. Bourianoff, and H. A. Atwater, *Nat. Mater.* **4**, 143 (2005).
- ⁶G.-R. Lin, C.-J. Lin, and C.-T. Lin, *Nanotechnology* **18**, 395202 (2007); G.-R. Lin, C.-J. Lin, and H.-C. Kuo, *Appl. Phys. Lett.* **91**, 093122 (2007); G.-R. Lin and C.-J. Lin, *ibid.* **91**, 072103 (2007).
- ⁷L. Dal Negro, J. H. Yi, J. Michel, L. C. Kimerling, S. Hamel, A. Williamson, and G. Galli, *IEEE J. Sel. Top. Quantum Electron.* **12**, 1628 (2006).
- ⁸P. Bellutti, L. Eccel, and N. Zorzi, *Microelectron. Reliab.* **40**, 747 (2000).
- ⁹Y. Liu, T. P. Chen, L. Ding, M. Yang, J. I. Wong, C. Y. Ng, S. F. Yu, Z. X. Li, C. Yuen, F. R. Zhu, M. C. Tan, and S. Fung, *J. Appl. Phys.* **101**, 104306 (2007).
- ¹⁰F. Jimenez-Molinos, F. Gamiz, A. Palma, P. Cartujo, and J. A. Lopez-Villanueva, *J. Appl. Phys.* **91**, 5116 (2002).
- ¹¹M. Barozzi, E. Iacob, L. Vanzetti, M. Bersani, M. Anderle, G. Pucker, and C. Kompocholis, *Rev. Adv. Mater. Sci.* **15**, 56 (2007).
- ¹²J. R. Yeargan and H. L. Taylor, *J. Appl. Phys.* **39**, 5600 (1968).
- ¹³M. P. Houng, Y. H. Wang, and W. J. Chang, *J. Appl. Phys.* **86**, 1488 (1999).
- ¹⁴C. I. Lee, V. H. Ngo, and D. S. Pan, *Appl. Phys. Lett.* **89**, 172112 (2006).
- ¹⁵Y. Ishikawa, M. Kosugi, M. Kumezawa, T. Tsuchiya, and M. Tabe, *Thin Solid Films* **369**, 69 (2000).
- ¹⁶J. Shi, L. Wu, X. Huang, J. Liu, Z. Ma, W. Li, X. Li, J. Xu, D. Wu, A. Li, and K. Chen, *Solid State Commun.* **123**, 437 (2002).
- ¹⁷D. N. Kouvatsos, V. Ioannou-Sougleridis, and A. G. Nassiopoulou, *Appl. Phys. Lett.* **82**, 397 (2003).
- ¹⁸R. Wetzler, A. Wacker, E. Scholl, C. M. A. Kapteyn, R. Heitz, and D. Bimberg, *Appl. Phys. Lett.* **77**, 1671 (2000).
- ¹⁹E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, New York, 1982).
- ²⁰E. P. Gusev, H.-C. Lu, E. L. Garfunkel, T. Gustafsson, and M. L. Green, *IBM J. Res. Dev.* **43**, 265 (1999).
- ²¹T. Z. Lu, M. Alexe, R. Scholz, V. Talalaev, R. J. Zhang, and M. Zacharias, *J. Appl. Phys.* **100**, 014310 (2006).
- ²²Z. Gaburro, G. Pucker, P. Bellutti, and L. Pavesi, *Solid State Commun.* **114**, 33 (2000).
- ²³A. G. Chynoweth and K. G. McKay, *Phys. Rev.* **102**, 369 (1956).
- ²⁴R. Lockwood, A. Hryciw, and A. Meldrum, *Appl. Phys. Lett.* **89**, 263112 (2006).