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Light emission and floating gate memory characteristics of germanium nanocrystals

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We report Ge nanocrystals (NCs) based dual functional light emitting and metal insulator semiconductor (MIS) flash memory devices, fabricated by rf sputtering. Transmission electron micrographs revealed the formation of spherically shaped Ge NCs. We have observed broad electroluminescence (EL) around 760 nm, which is attributed to electron–hole recombination in quantum confined Ge NCs. The dependence of integrated EL intensity on drive currents has also been studied. An anti-clockwise hysteresis behaviour is observed in capacitance–voltage measurements of MIS devices for different sweep voltages, indicating net electron trapping in NC based floating gates.

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1 Introduction Multifunctional electronic devices are attractive since one device can play a role of two or more. Light emitting diodes solar cells, light emitting transistors and light emitting memory devices [1] are representative dual functional devices. Nanocrystal (NC) light emitting memory devices have dual functions of MOS light emitting diodes and floating gate memory behaviour. In NCs floating gate devices, metal or semiconductor NCs are embedded as charge-storage nodes in an oxide layer between the control gate and the tunnelling layer to replace the continuous floating gate layers in conventional flash memories [1–3]. The use of NCs as floating gates offers smaller operating voltages, better endurance characteristics and faster write/erase speeds as compared to conventional flash memories [4, 5]. Due to the smaller band-gap, superior carrier mobilities and higher excitonic Bohr radius compared to Si, Ge NCs are considered to be ideal nodes for use in complementary metal oxide semiconductor compatible memory circuits. On the other hand, persistent efforts have been made to achieve efficient light emission from silicon–germanium NCs, in order to extend the use of silicon technology into fully integrated optoelectronic circuits, meeting the requirements for high-bandwidth intrachip and interchip connects [6]. Light emission in bulk silicon-based devices is constrained in wavelength to infrared region and in efficiency by the indirect bandgap of silicon. Enhanced light emission from silicon is predicted to be theoretically possible [7], enabled mostly through quantum-confinement effects [8, 9]. There are only few reports on Ge NCs based LED [10, 11]. One of the main problems of LED based on Ge NCs in oxide matrix is the carrier injection. The light emission from these MOS devices is explained by (i) impact ionization of NCs by hot electron injection into the oxide matrix under a high-electric field or (ii) co-tunnelling of carriers into NCs from both side of the devices.

In this paper, we report the fabrication of Ge NCs dual functional light emitting metal insulator semiconductor (MIS) based flash memory devices by rf sputtering. We have studied the light emission and charge trapping behaviour of Al/HfO_2/HfO_2 + Ge-NCs/HfO_2/Si MIS structure. Observed polarity dependent light emission in the electroluminescence (EL) measurements is attributed to the co-tunnelling of electrons and holes into the NCs embedded in HfO_2 matrix rather than impact ionization. An anti-clockwise hysteresis behaviour is observed in capacitance–voltage (*C*–*V*) measurements for different sweep voltages, indicating net electron trapping in NCs. By using a high-*k* dielectric in place of SiO_2, a larger tunnelling current is achieved in MIS LEDs due to the lower

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electron barrier height of HfO_2 (1.2 eV) [12] as compared to SiO_2 (3.1 eV). Furthermore, momentum conservation in radiative process is facilitated by soft phonon scattering in high-*k* dielectrics [13].

2 Experimental

The light emitting memory structures used in this study was MOS capacitors with a dielectric stack consisting of Ge NCs sandwiched between tunnelling and capping layers of HfO_2. P-type (100) Si substrates with resistivity 7–14 Ω cm, were initially cleaned by Piranha process followed by dipping in dilute HF for 1 min to remove the native oxide from the surface. First a thin tunnelling layer of HfO_2 (∼4 nm) was deposited on Si by rf magnetron sputtering technique from a 3 in. dia. HfO_2 (99.999% pure) target at 50 W rf power for 8 min in Ar + O_2 ambient. The intermediate layer was then deposited by co-sputtering of HfO_2 and Ge for 20 min under the same condition, with a volume ratio of HfO_2:Ge = 85:15.Finally a cap layer of HfO_2 was deposited at a 50 W rf power for 40 min in Ar + O_2 ambient. The trilayer structure was then subjected to thermal annealing in nitrogen at 850 °C for 30 min. A thin semi-transparent Al-gate top electrode (area: 1.96×10^{-3} cm^2) and a large area Al bottom contact at the back of the device were made by thermal evaporation followed by a low temperature thermal annealing for few minutes.

High-resolution transmission electron microscopy (HRTEM) was carried out using a JEM 2100F (JEOL) system with an operating voltage of 200 kV to study the microstructural properties of Ge NCs in the trilayer structure. The electrical properties of the trilayer structure were obtained using a Keithley semiconductor parameter analyser. The EL was collected with a Spectra-Pro 2300i monochromator coupled with a nitrogen cooled charge coupled device (CCD) camera. The total light intensity was then calculated by integrating the CCD camera signal over the illuminated pixels. The measurements were performed at room temperature in dark condition.

3 Results and discussion

3.1 Formation of Ge nanocrystals

Figure 1 shows a plain-view transmission electron micrograph of sample annealed at 850 °C for 30 min in N_2 atmosphere. The dark patches are Ge NCs of 4–9 nm diameter in the HfO_2 matrix. The NCs are almost spherical and are well dispersed in the HfO_2 matrix. The inset of Fig. 1 shows the HRTEM image of one such NC, which exhibit clear lattice fringes. The average diameter of the NC is about 6.5 nm. The change in Gibbs free energy of formation (at 298.15 K) of GeO (−111.8 kcal/mol) [14] is much smaller than that of high-*k* HfO_2 (−260.1 kcal/mol). There for the change in Gibbs free energy (ΔG) is negative in solid reaction of $GeO_2 + Hf \rightarrow HfO_2 + Ge$. Hence the mixture of HfO_2 and Ge has the lower Gibbs free energy in the co-sputtered film, resulting in the agglomeration of Ge atoms into NCs.

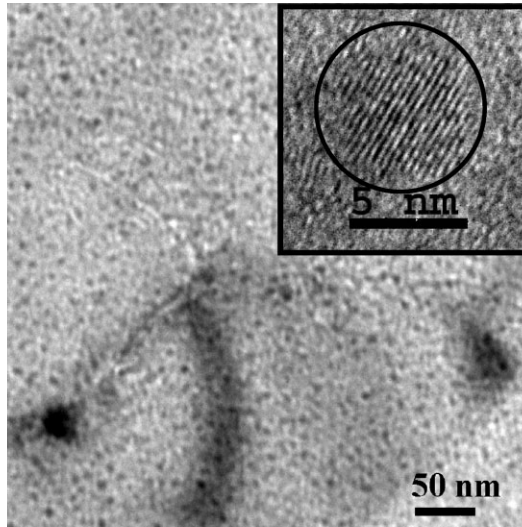

Figure 1 Plain-view TEM micrograph of Ge NCs embedded in HfO_2 matrix. Dark patches are NCs. Inset shows the lattice fringes of one such NC.

3.2 Electrical conduction

As Ge/Si is an indirect gap semiconductor, the preparation of Si-based LED diodes is one of the main challenges of silicon microelectronics technology for the fabrication of optoelectronic devices. EL has been widely studied in MIS structures fabricated on Si with Si/Ge NCs embedded in the dielectric layer [1, 8–11, 15]. A critical challenge for the MOS LED based on NCs embedded in oxide has been the development of a method for efficient carrier injection. Under the positive gate bias, electron current from the Si conduction band is enhanced using high-*k* HfO_2 as a blocking oxide. While in the −ve gate bias, the hole injection from the Si valance band can be enhanced and the electron current from the gate electrode can be suppressed using high-*k* HfO_2 as a blocking oxide. To get a high-program/erase speed, the difference between electron and hole current should be higher. Figure 2 presents the current versus voltage (*I*–*V*) characteristics of the memory

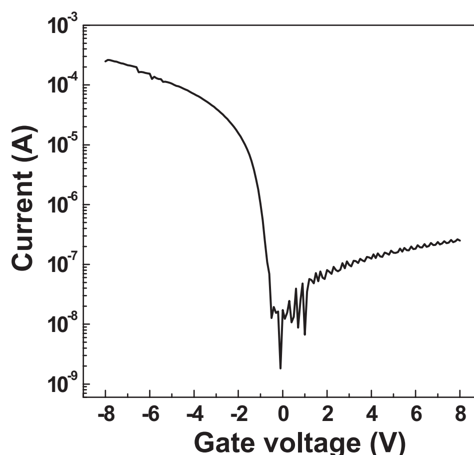

Figure 2 Current–voltage characteristics of the MOS capacitor with Ge NC in high-*k* HfO_2 matrix.

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structure. The tunnelling effect owing to NCs is clearly seen in both accumulation and inversion, when the *I–V* curve bends over in the intermediate voltage region and the current increases slowly for voltages up to 8 V. The detailed tunnelling mechanisms through high-dielectric permittivity materials are still under investigation. Fowler–Nordheim (F–N) tunnelling, direct tunnelling and Frenkel–Poole tunnelling (F–P) have been proposed to explain the experimental results at various voltage ranges [12, 16]. It is also well known that the F–N tunnelling current is higher, when it is due to the majority carriers and relatively weak if it is due to the minority carriers. In our device we have also seen that for higher electric field the tunnelling current in the accumulation regime (majority carrier) is higher than that of inversion regime (minority carrier). It may be noted that a low backward tunnelling current, thin tunnelling oxide and small valence band offset between the trapping layer and Si substrate are necessary for easy erasing of stored charges from the floating gate. During this erase mode, a negative voltage is applied at the gate. A small valence band offset between the trapping layer and p-Si enhances the hole tunnelling [17], which would recombine with the stored electrons within the NCs for the erase operation.

3.3 Electroluminescence behaviour The MOS structure containing Ge NCs embedded in HfO_2 shows EL at room temperature. The EL spectra are dependent on the polarity of the potential bias and emission was observed only under negative gate bias. Figure 3 shows the integrated EL (I_{EL}) from the device as a function of current density (J). The curve is plotted in double-logarithmic scale. The EL onset voltage of the device is about −13 V. The $I_{EL} - J$ characteristics posses a power law, i.e. $I_{EL} \sim J^{\alpha}$, with α being 0.97. This indicates a nearly linear dependence of EL intensity on injection current. The EL spectra collected at the injected currents of 9.8, 15 and 18 mA are shown in Fig. 4. The spectra show a broad EL in the visible and near infrared region. The EL peak (18 mA) can be deconvoluted by three Gaussian peaks with peak position centred at 644, 760 and 898 nm with FWHM of 85, 113 and 79 nm, respectively.

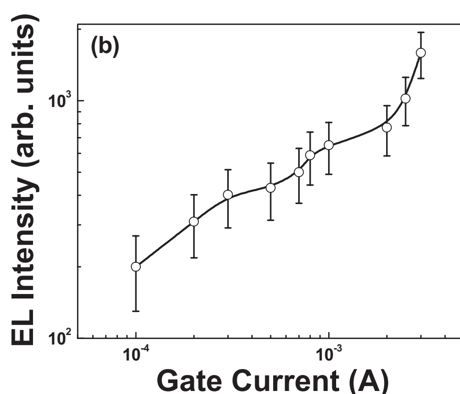

Figure 3 Integrated EL intensity as a function of the injected current.

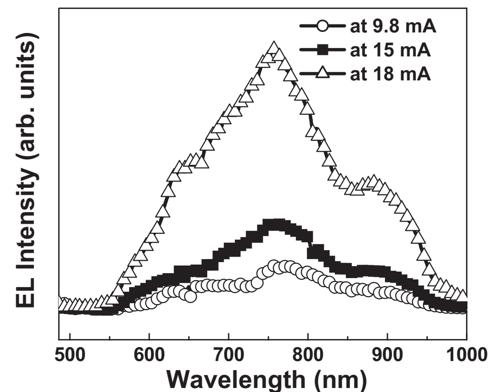

Figure 4 EL spectra at the injected currents of 9.8, 15 and 18 mA. The spectra are normalized for spectrograph response.

Using simple confinement model [2], the 760 nm EL peaks corresponds to 6.9 nm Ge particle size, which closely matches with the observed one obtained from the TEM micrograph. Therefore the intense EL peaks at 760 nm can be attributed to electron–hole recombination in the Ge NCs. On the other hand, 644 nm emission is far away from the quantum confined effect of 6.5 nm Ge NCs. There are several reports of luminescence in the blue–green region with the peak energy independent of the size of the NCs [18]. Therefore the observed emission band around 644 nm originates due to radiative recombination through defects, which are located at the interface of the NCs. Another weake EL peaks at 898 nm is attributed to the oxygen related defects in GeO_2. It may be noted that, the EL is observed only for forward bias condition with negative voltage at the metal gate. Therefore the observed emission is attributed to the radiative recombination of tunnelled electrons from gate electrode and holes from p-type Si into the Ge NCs located inside the HfO_2 matrix rather than the impact ionization that might take place in the NCs.

3.4 Charge injection and retention characteristics *C–V* measurement of memory capacitors has been an attractive method of obtaining device characteristics due to the ease of experimental setup and data analysis. Figure 5 shows the high-frequency (1 MHz) *C–V* curves for the sample with Ge NCs embedded in HfO_2 matrix for different sweep voltages. An anti-clockwise hysteresis characteristics is observed for the Ge NC try-layer device indicating net electron trapping in the Ge-NCs embedded sandwich structure. A very small flat-band voltage shift of 0.13 V is observed for the control sample without Ge NCs. This suggests that the origin of *C–V* hysteresis can be attributed to injected charges mainly in NCs or at the interfaces between the NCs and the surrounding oxides, rather than the traps in HfO_2. For ±7 V sweep voltage a flat-band voltage shift of 4.85 V for NC-MOS devices give rise to a stored charge density (N_{charge}) of $1.07 \times 10^{13}\,cm^{-2}$

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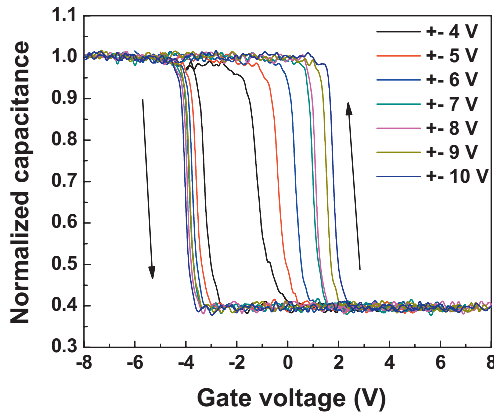

Figure 5 (online colour at: www.pss-a.com) High-frequency (1 MHz) *C–V* characteristics of MOS capacitor with Ge NCs in high-*k* HfO_2 matrix for different sweep voltages.

using [19]

$$N_{\text{charge}} = \frac{\Delta V_{\text{FB}}}{\frac{q}{\varepsilon_0}\left(\frac{t_{\text{CO}}}{\varepsilon_{\text{CO}}} + \frac{t_{\text{NC}}}{\varepsilon_{\text{NC}}}\right)}, \quad (1)$$

where ΔV_{FB} is the flat-band voltage shift, q the magnitude of the electronic charge; t_{CO} and ε_{CO} are the thickness and relative permittivity of the control oxide; t_{NC} and ε_{NC} are the diameter and relative permittivity of the NC; and ε_0 is the permittivity of the free space.

Figure 6 shows the charge retention characteristics of the Ge NCs nonvolatile memory capacitor. At first, the memory capacitor was programmed under a drive gate voltage of +7 V for 1 s. Then, the V_{FB} was measured with time. Similarly, the memory capacitor was erased under a drive gate voltage of −7 V for 1 s and the V_{FB} was measured with time. Assuming logarithmic behaviour for retention, the extrapolation of V_{FB} shift for memory capacitor has been performed up to 10 years. The memory windows of the device estimated to be 3.03 V at 25 °C after 10 years of retention with charge losses of the memory is estimated to be 37%. Due to the large memory window and low charge loss of the Ge NCs memory device with high-*k* HfO_2 as a blocking oxide and a high-work function metal gate, it can be used in future high-density and scaled flash memory device applications.

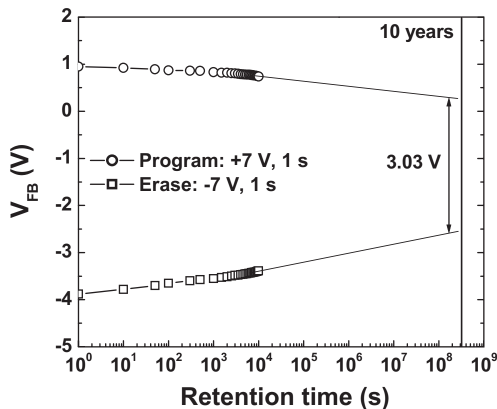

Figure 6 Retention characteristics of the Ge NCs memory device.

4 Conclusions

We have demonstrated the light emission and charge trapping behaviour of Al/HfO_2/Ge-NCs/HfO_2/Si MIS structures. Observed broad EL around 760 nm is attributed to the electron–hole recombination in quantum confined Ge NCs. An anti-clockwise hysteresis behaviour is observed in *C–V* measurements of MIS devices for different sweep voltages, indicating net electron trapping in NC based floating gates.

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